**FPGA vs. ASIC in Satellite Embedded Systems with Power Subsystems and Sensor Multiplexing.**

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# Abstract

Embedded systems in satellites must handle mission-critical tasks such as real-time data processing, communication, and power management, all while operating under the extreme conditions of space. Two of the primary hardware solutions for these functions are Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs). FPGAs offer flexibility and reconfigurability, which are essential for adapting to changing mission requirements or fixing issues post-launch, but they typically consume more power than ASICs. In contrast, ASICs provide high performance and power efficiency, as they are custom-designed for specific tasks, but they lack the reconfigurability that FPGAs offer.

This paper analyzes these trade-offs, comparing FPGA and ASIC solutions in the context of satellite embedded systems. It delves into the advantages and challenges associated with each, highlighting performance, power efficiency, and reconfigurability as key considerations. Furthermore, the paper examines the role of power subsystems and multiplexing techniques for managing analog sensors in satellite systems, which are crucial for optimizing overall satellite design and ensuring that the system can operate efficiently in space.

*Keywords—FPGA, ASIC, satellite systems, embedded systems, power subsystem, sensor multiplexing, reconfigurability, performance, power efficiency*

# Introduction

This research paper examines the pivotal roles of Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) in satellite embedded systems, focusing on their integration within power subsystems and sensor multiplexing. As space missions become more advanced and the demands on satellite systems increase, the need for high-performance, power-efficient, and reliable embedded systems has never been more urgent. In the challenging environment of space, satellites must handle a wide range of tasks, including real-time data processing, signal routing, and efficient power management, all while operating under extreme conditions such as high radiation and fluctuating temperatures.

The choice of hardware in satellite systems is a major factor in determining overall system performance, power consumption, and flexibility. FPGAs, known for their flexibility and parallel processing capabilities, are highly suitable for tasks that require frequent updates or adaptations throughout a mission. These capabilities allow satellites to adapt to new challenges or unexpected conditions during their operation. For instance, FPGAs can reconfigure themselves to handle new data formats or change their processing logic in response to evolving mission requirements. This reconfigurability gives FPGAs an edge in dynamic mission environments where adaptability is crucial.

In contrast, ASICs, while not as flexible as FPGAs, provide highly optimized solutions for fixed tasks, delivering unparalleled performance with minimal power consumption. This makes them an excellent choice for tasks that require high reliability and consistent performance, such as sensor data acquisition or specific signal processing functions. ASICs are custom-designed to perform specific tasks efficiently, which allows them to operate with significantly lower power usage, an important consideration in the resource-constrained environment of space.

This paper compares and contrasts these two hardware solutions, focusing on their application in satellite power subsystems and sensor multiplexing. It examines the advantages and limitations of both technologies when used in space applications, considering aspects such as power efficiency, reliability, and scalability. The research also discusses the challenges of integrating FPGA and ASIC technologies within the constraints of space missions, offering insights into how a hybrid approach could potentially leverage the strengths of both technologies. By combining the adaptability of FPGAs with the power efficiency and reliability of ASICs, satellite systems could achieve an optimal balance of performance, flexibility, and power management.

The goal of this paper is to provide a comprehensive and insightful analysis of FPGA and ASIC technologies as they pertain to satellite embedded systems. It explores how these technologies can help optimize satellite performance while addressing the unique challenges of operating in space. As we look toward the future of space exploration, it is clear that the right combination of hardware will be crucial in enabling satellites to perform at their best, efficiently utilizing available resources and adapting to the demands of increasingly complex missions.

This research aims to contribute to that understanding by shedding light on how FPGA and ASIC technologies are shaping the future of satellite systems and the possibilities they offer for next-generation space missions.

# Overview of the Power Subsystem (EPS) in Satellite Embedded Systems: A Hybrid Approach

In satellite embedded systems, the Power Subsystem (EPS) plays a critical role in managing and distributing power across the satellite.

Given the unique challenges of space, where power resources are limited and conditions can change rapidly, ensuring efficient power management is crucial for the success of a mission. Space environments demand a system that not only maximizes power efficiency but also adapts to fluctuating conditions.

To address these challenges, we explored a hybrid approach combining Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs). FPGAs provide flexibility and adaptability, enabling the system to reconfigure itself in response to changing mission needs or unforeseen environmental factors. This reconfigurability is particularly beneficial in space, where the ability to quickly adjust to new data or power management requirements can make a significant difference.

Meanwhile, ASICs offer optimized, fixed solutions for specific tasks, providing excellent power efficiency and reliability. By using ASICs for key power regulation functions, the EPS can achieve high performance with minimal power consumption. This hybrid FPGA-ASIC approach combines the adaptability of FPGAs with the power-saving capabilities of ASICs, making it an ideal solution for optimizing the EPS.

This approach ensures that satellite power subsystems remain efficient, adaptable, and resilient in the ever-changing conditions of space.

## A. Understanding the Hybrid Approach

The hybrid approach represents a smart fusion of Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) within a single system, carefully designed to harness the unique strengths of both technologies. In this setup, FPGAs bring unmatched flexibility and the ability to process data in real-time, which is essential when the system needs to adapt dynamically to unforeseen circumstances or changing conditions.

On the other hand, ASICs are purpose-built for specific tasks, offering high efficiency and superior performance for fixed, repetitive operations that require minimal power.

By strategically assigning tasks to the most suitable technology—using FPGAs for tasks that require quick adjustments or real-time data processing, and relying on ASICs for power-efficient, fixed tasks—we aimed to build a power subsystem that delivers both adaptability and efficiency. This hybrid system is designed to ensure that the satellite performs optimally under the demanding and unpredictable conditions of space, where variables like solar exposure can change rapidly, and where the efficient management of battery storage is a constant challenge.

In the extreme environment of space, where resources are limited and performance reliability is critical, this hybrid approach ensures that the satellite’s power subsystem not only meets the power demands of the mission but also responds to any changes that might arise.

Whether it's fluctuating energy availability due to varying solar exposure or the constant need for efficient power storage management, the combination of FPGAs and ASICs ensures that the satellite can operate effectively, adapting to the conditions without compromising performance. This thoughtful balance of flexibility and power efficiency is key to ensuring the satellite can endure the harsh realities of space while meeting its mission goals.

*B. Implementation of the Hybrid Approach in Power Subsystems*

The first step in implementing the hybrid approach involved carefully identifying which tasks within the Power Subsystem (EPS) would benefit most from the unique strengths of both FPGA and ASIC technologies. This allowed us to allocate responsibilities efficiently, ensuring that each component was tasked with what it does best.

**Figured 1**: Power Efficiency Comparison: FPGA vs ASIC [17]

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The chart below highlights the power efficiency comparison between FPGA and ASIC, emphasizing how ASICs provide superior energy efficiency for fixed tasks, whereas FPGAs, although more flexible, consume more power in comparison.

Here’s a closer look at how we divided the tasks to maximize both flexibility and power efficiency:

1. FPGA for Real-Time Power Management:

The FPGA was entrusted with managing real-time power adjustments, a critical role in satellite operations where environmental conditions can change rapidly. Its reconfigurability gave us the ability to adapt the system’s power management strategy in real time.

For instance, when the satellite enters the Earth’s shadow, the FPGA could adjust the power distribution to ensure that essential systems, like communication and navigation, continued to operate smoothly despite the lack of sunlight.

Similarly, as the satellite’s orbit changes, so does the angle of sunlight it receives, and the FPGA dynamically adapts the power distribution to account for these variations. This constant real-time adjustment is essential in ensuring that power is available when and where it’s needed most.

In addition to this, the FPGA was also responsible for dynamic power routing to different subsystems, based on their varying power requirements. By continuously monitoring the satellite’s systems, it ensured that critical systems always received the necessary power while preventing overloading by other less critical components.

This intelligent power routing helped maintain overall system stability, ensuring the satellite could continue performing its tasks without exceeding power capacity.

1. ASIC for Power Efficiency:

While the FPGA handled the dynamic and adaptable aspects of power management, the ASICs took care of the repetitive, fixed functions that didn’t require real-time adjustments but demanded efficiency and reliability. For example, the ASICs were responsible for voltage regulation, ensuring that every subsystem received a stable, consistent voltage. This was especially important in space, where fluctuations in power supply are inevitable, and providing each system with the correct voltage is vital to maintaining their functionality.

Another key task managed by the ASICs was battery charging. This task is central to maintaining the satellite’s power storage system, ensuring the battery is charged in the most efficient way possible while protecting it from overcharging or deep discharges.

Since these are repetitive, predictable tasks, ASICs are ideally suited to handle them with minimal power consumption, making them a more energy-efficient choice compared to FPGAs. Their ability to perform these functions efficiently was crucial in preventing unnecessary energy loss and helping to conserve the satellite’s power reserves for the long-term duration of the mission.

1. Hybrid Power Distribution:

To make the most of both FPGA and ASIC capabilities, we designed the Power Distribution Module (PDM) to work in harmony with both components. The FPGA continuously monitored the real-time power consumption of various subsystems, gathering data on how much power each one required at any given moment.

This allowed the FPGA to communicate with the PDM and adjust power allocation dynamically, ensuring that each subsystem received the optimal amount of power based on its real-time demands. If a subsystem required more power to complete a critical task, the FPGA could reroute the power supply accordingly.

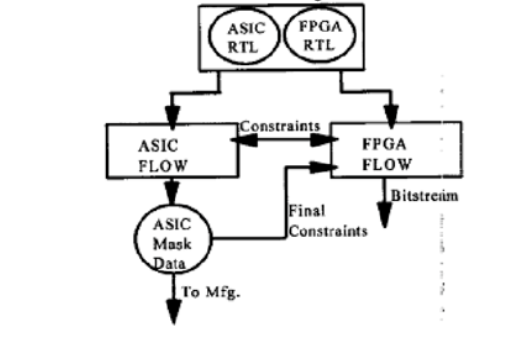
Meanwhile, the ASICs ensured that the power supply remained stable and consistent. By handling voltage regulation, the ASICs ensured that no subsystem would receive too much or too little power, keeping everything within safe operating limits.

This balance between dynamic power adjustments handled by the FPGA and consistent power regulation managed by the ASICs created a well-optimized system, able to deal with the unpredictable nature of space while maintaining high performance.

## C. Findings of the Hybrid Approach

Through our implementation of the hybrid FPGA-ASIC approach, we made several key observations that underscored the effectiveness of combining the strengths of both technologies in optimizing satellite power management.

**Figure 2:** Hybrid FPGA-ASIC Integration in Power Subsystems, referenced in [16]



This diagram highlights the seamless integration of FPGA and ASIC components within a hybrid system, designed to optimize power management in satellite embedded systems. It shows how each component plays a distinct but complementary role. The FPGA takes charge of real-time tasks, such as dynamically adjusting power distribution and processing telemetry data, allowing the satellite to adapt to changes in its environment instantly.

Meanwhile, the ASIC handles more fixed, stable operations, like regulating voltage and managing battery efficiency, ensuring that the power system remains steady and reliable over time. The flow between these two technologies is shown in the diagram, illustrating how they work together—balancing flexibility and stability. This hybrid approach allows the satellite to effectively manage varying power conditions, ensuring smooth and continuous operation, even in the challenging environment of space.

1. Real-Time Adaptability:

One of the standout features of the FPGA was its ability to reconfigure in real-time, providing dynamic power management based on the satellite’s immediate needs. For example, when the satellite entered an eclipse phase—where solar power was unavailable—the FPGA seamlessly adjusted power distribution from the batteries to ensure continued operation.

This adjustment was done without any need for human intervention, illustrating the FPGA’s ability to respond autonomously to changing conditions. The reconfigurability of the FPGA proved invaluable in maintaining system stability and ensuring that the satellite’s essential functions could continue uninterrupted, even in the face of fluctuating environmental factors.

1. Improved Power Efficiency:

The ASICs, with their fixed functionality, proved to be much more power-efficient than the FPGAs for tasks that didn't require reconfiguration. Functions like voltage regulation and battery management—both of which are essential for maintaining a stable power supply to the satellite’s subsystems—were managed effectively by the ASICs. Because these tasks are repetitive and predictable, the ASICs excelled in delivering high performance while consuming significantly less power.

This power-saving aspect of the ASICs helped extend the overall operational lifetime of the satellite by reducing unnecessary energy consumption, allowing the satellite to optimize its use of limited resources.

1. Increased System Reliability:

By leveraging the unique strengths of both FPGA and ASIC, the hybrid approach contributed to a more reliable power subsystem. The ASICs ensured that critical functions like voltage regulation were handled with precision and consistency, minimizing the risk of failure.

These tasks, which require high stability and low error tolerance, benefited from the ASIC’s dedicated, optimized design. Meanwhile, the FPGA was responsible for handling more complex tasks, such as real-time power management and adaptability to changing conditions.

Together, these two technologies provided a solid foundation for the satellite’s power subsystem, ensuring it remained operational under both predictable and unexpected circumstances.

1. Optimized Power Allocation:

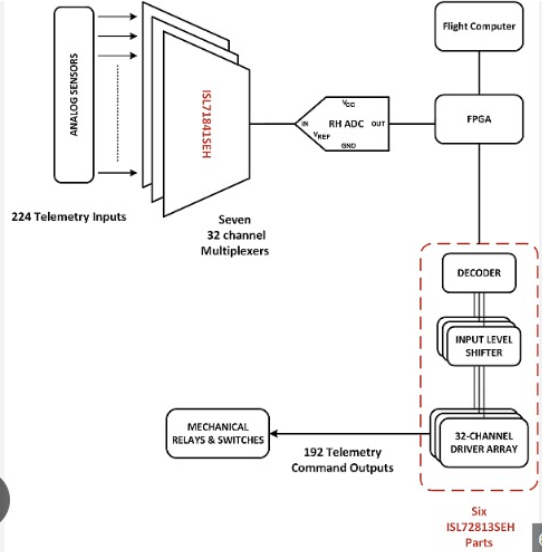
The hybrid system also allowed for optimized power allocation throughout the satellite. The FPGA’s real-time monitoring capabilities enabled it to prioritize subsystems that required the most power at any given time, ensuring that the satellite’s energy resources were used in the most efficient way possible.

For example, during non-critical periods, the FPGA could adjust power usage to conserve energy, ensuring that the battery lasted longer. Conversely, during high-priority tasks, like communication or sensor operations, the FPGA could allocate the necessary power to those subsystems, making sure they functioned without delay. This intelligent, adaptable power management significantly improved the satellite’s efficiency and ensured that it could meet the demands of its mission while maintaining optimal power usage.

In summary, the hybrid FPGA-ASIC approach provided a balance of flexibility, efficiency, and reliability, ensuring that the satellite’s power subsystem could adapt to the challenges of space while remaining power-efficient and resilient. This dual-technology solution not only maximized performance but also optimized power usage, making the satellite more capable of withstanding the rigors of space operations.

# Overview power Subsystem hardware

**Figure 3:** Overview of Power Subsystem Hardware**.** Referenced in [15]



This figure provides a comprehensive overview of the power subsystem hardware in a satellite system, with a particular focus on how key components work together to manage power generation, storage, and distribution.

It highlights the essential elements that make up the Power Subsystem, such as the solar panels, battery storage, DC-DC converters, and the Power Distribution Module (PDM). Each of these components is crucial in ensuring the satellite operates efficiently by maintaining a steady flow of power to its subsystems, even when solar generation is low or during eclipse phases when the satellite is in the Earth's shadow.

The Power Subsystem is intricately integrated with the hybrid FPGA-ASIC approach, which we implemented in our research to enhance the power management process. This hybrid system combines the flexibility of FPGAs with the efficiency of ASICs, enabling real-time adjustments to power distribution based on the satellite’s immediate needs. The FPGA manages the dynamic aspects of power routing, ensuring that energy is distributed efficiently across the satellite’s subsystems. Meanwhile, the ASICs handle fixed tasks such as voltage regulation and battery management, ensuring that power remains stable and efficient.

Together, these technologies ensure that the satellite’s power system not only meets the demands of its operations but does so with maximum efficiency, adapting to changing conditions and conserving energy when possible.

## A. Power Subsystem and Hybrid FPGA-ASIC Approach

1. FPGA's Role in Power Management:

* The FPGA plays an essential role in managing power dynamically and in real-time, ensuring the satellite’s power system adapts smoothly to changing conditions. In Figure 1, the FPGA interacts with key components such as the solar panels, battery, and DC-DC converters to control the distribution of power throughout the satellite.
* Thanks to the FPGA’s parallel processing capabilities, it can manage multiple power sources at once, adjusting the power flow to various subsystems based on their fluctuating needs. This becomes especially critical when solar generation is inconsistent or when the satellite enters an eclipse phase, where it no longer receives direct sunlight. The FPGA continuously monitors and adapts to the satellite’s needs, adjusting power distribution to ensure that every subsystem gets the necessary energy without overloading the system. Its ability to handle real-time, dynamic changes ensures that the satellite stays operational even in the face of unpredictable space conditions.

2. ASIC's Role in Power Subsystem:

* On the other hand, the ASIC is dedicated to handling fixed, stable tasks that don't require constant reconfiguration but are crucial for the satellite’s steady operation. As shown in the figure, ASICs manage essential functions like voltage regulation and battery management—key tasks for ensuring that power remains stable and reliable across the satellite's subsystems.
* These functions are repetitive and predictable, making them ideal for the efficiency of ASICs, which are designed to perform them with minimal power consumption while maintaining high reliability. The ASIC ensures that power is delivered efficiently by managing the DC-DC converters and overseeing the battery’s health and charging process. By offloading these crucial tasks to ASIC, the power system becomes much more stable, reducing the risk of power wastage or supply interruptions. This stability is especially important in long-term satellite missions, where continuous, reliable power is critical to maintaining all systems operational.

# Architecture

#### **Hardware**

#### The hardware architecture of the Electrical Power Subsystem (EPS) in satellite embedded systems serves as the foundation for real-time power management, distribution, and environmental monitoring. This system is engineered to operate reliably under the extreme conditions of space, including radiation exposure, thermal fluctuations, and constrained energy availability.

#### The EPS includes core components such as solar panels for energy harvesting, batteries for storage during eclipse periods, DC-DC converters for voltage regulation, and Power Distribution Modules (PDMs) for routing power to subsystems. Control logic is implemented through a hybrid FPGA-ASIC design, which enables the system to maintain both flexibility and energy efficiency.

## Hybrid FPGA-ASIC Integration

#### At the heart of this architecture lies a hybrid model that combines the reconfigurability of FPGAs with the power efficiency of ASICs. The FPGA (Field-Programmable Gate Array) is used to handle dynamic, real-time decision-making tasks, such as adapting power flow in response to changing environmental conditions or shifting subsystem demands. The ASIC (Application-Specific Integrated Circuit), on the other hand, performs fixed, low-power functions such as voltage regulation and battery management, where stability and energy efficiency are paramount. This division of responsibilities ensures optimal use of hardware resources: the FPGA enables adaptive control during mission-critical transitions—like eclipse entry or load spikes—while the ASIC guarantees consistent performance for routine operations.

## Sensor Multiplexer Implementation (FPGA)

#### To enable efficient sensor data acquisition without exhausting input/output resources, a VHDL-based sensor multiplexer (MUX) was implemented on the FPGA. This MUX allows the system to select among multiple analog inputs—such as voltage, current, temperature, and battery sensors—using a 2-bit selector signal. Instead of dedicating separate ADCs or input pins for each sensor, the MUX dynamically routes one signal at a time to a shared analog-to-digital converter (ADC).

#### This approach significantly reduces hardware complexity, lowers power consumption, and enables real-time environmental monitoring across key EPS components.

#### **Figure 4:** VHDL code of the 4-to-1 Sensor MUX

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#### A close up of a circuit board AI-generated content may be incorrect.

#### The y output of the MUX delivers the selected sensor’s signal to the ADC, where it is digitized and processed by the FPGA’s control logic. This selective monitoring capability allows the system to focus on the most relevant sensor data at any given moment, which is especially critical for intelligent power allocation and fault response in space.

## Environmental Sensing and Monitoring

#### To maintain operational stability and prolong the satellite's lifespan, the system incorporates high-precision sensors for monitoring power and thermal conditions. Voltage and current sensors are deployed at key locations, including solar panels, battery terminals, and power buses, to measure energy generation and consumption. Temperature sensors provide real-time feedback on thermal performance, ensuring components remain within safe operating limits.

#### The FPGA continuously processes this telemetry data, enabling real-time power allocation and early fault detection. This sensing layer, combined with the multiplexer, forms a scalable and power-efficient telemetry system that supports adaptive control and predictive diagnostics.

#### D. Protection and Interface Design

#### To ensure operational safety, the system integrates protection circuits capable of autonomously responding to critical events such as overvoltage, overcurrent, or thermal overload. These circuits are designed to isolate faulty subsystems and preserve mission-critical functionality. Additionally, the system includes communication interfaces, such as CAN bus or SpaceWire, to transmit real-time telemetry between the EPS and other satellite systems.

## Power Conditioning and Isolation

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#### The EPS employs isolated DC-DC converters to deliver stable, regulated voltage to the FPGA, ASIC, and other sensitive control components. Galvanic isolation techniques—including optocouplers and isolated transformers—are used to protect the system from electrical disturbances, ensuring reliable operation under all mission conditions.

## Protection and Communication

#### Ensuring operational safety in space requires the power subsystem to autonomously respond to hazardous events without delay. Protection circuits are embedded within the system to detect and mitigate conditions such as overvoltage, undervoltage, and thermal anomalies. These circuits operate independently from the main control processor, enabling immediate protective actions—such as isolating faulty components—to prevent system-wide failures.

#### Reliable communication between the EPS and other satellite subsystems is essential for coordinated control. The hardware architecture integrates robust communication interfaces, such as Controller Area Network (CAN) and SpaceWire protocols, to transmit telemetry data and control signals between the FPGA, ASIC, and other onboard systems. These protocols offer high-speed, fault-tolerant communication, enabling synchronized operation across the satellite.

#### G. Power Management and Isolation

#### The EPS incorporates a dedicated power management subsystem to deliver clean, stable power to the FPGA, ASICs, sensors, and control units. This is achieved through isolated DC-DC converters, which step down energy from the main battery pack into precise voltage levels required by sensitive digital components. By isolating power domains, the system minimizes the risk of noise or voltage fluctuations disrupting critical operations.

#### To enhance fault tolerance, galvanic isolation methods—such as optocouplers and isolated transformers—are employed. These protect low-voltage control logic from high-voltage transients, safeguarding key circuits against power spikes. This layer of electrical isolation ensures long-term hardware integrity and operational reliability throughout the satellite’s mission.

## EPS Component Integration

#### **Figure 5:** Hardware Architecture of the Satellite Power Subsystem. Referenced in [14]

#### Uploaded image

#### The complete EPS architecture is a tightly integrated network of components, each playing a specific role in the collection, conversion, monitoring, and distribution of electrical power. The system includes multiplexers (MUX), analog-to-digital converters (ADC), general-purpose input/output (GPIO) pins, memory units, and a microcontroller (MCU) that coordinates subsystem control alongside the FPGA and ASIC components.

#### Multiplexers are used to manage sensor telemetry efficiently. In this design, 16:1 and 8:1 MUXes route signals from multiple sensors—monitoring voltage, current, and temperature—to the shared ADC channel. This reduces the number of required input pins and streamlines the hardware design, enabling the system to collect diverse environmental data without overloading the MCU or the FPGA.

#### The ADC converts these analog sensor readings into digital data, enabling accurate measurement of electrical and thermal metrics across the EPS. These values are then processed by the MCU and FPGA for real-time decision-making, fault detection, and dynamic power control.

#### GPIO pins are used to interface with actuators such as relays and switches that control power distribution. The FPGA or MCU can toggle these outputs based on telemetry data, enabling or disabling specific subsystems as needed to conserve energy or respond to faults.

#### Memory modules store system logs, configuration data, and telemetry history, ensuring the EPS can retain critical information even during periods of communication blackout. This stored data supports offline diagnostics and enhances mission resilience.

#### J. Hybrid Control: FPGA and ASIC Collaboration

#### The collaboration between FPGA and ASIC is central to the intelligence and efficiency of the EPS. The FPGA is responsible for time-sensitive and adaptive tasks, such as switching power sources during eclipse events, prioritizing power delivery to critical loads, and monitoring sensor trends. Its reprogrammable nature allows updates and logic reconfiguration even after deployment.

#### The ASIC complements the FPGA by handling routine, energy-critical operations like battery charging, voltage regulation, and fault isolation. ASICs provide speed and energy savings due to their fixed-function architecture, making them ideal for continuous background processes that do not require runtime changes.

#### This hybrid strategy allows the EPS to maintain a balance between flexibility and efficiency, ensuring that the satellite can adapt to dynamic space conditions while conserving power. The FPGA’s logic can respond to mission-phase-specific demands, while the ASIC sustains essential operations with minimal overhead.

## Conclusion of Hardware Section

#### The overall hardware design of the EPS leverages a robust combination of intelligent sensing, multiplexed signal routing, real-time processing, and autonomous protection. The VHDL-implemented sensor multiplexer, combined with the hybrid FPGA-ASIC architecture, exemplifies how smart digital logic and efficient analog support work together to build a resilient, adaptive power system for space applications. This integrated approach ensures that the satellite remains operational, efficient, and protected throughout the duration of its mission, even under the most challenging environmental conditions.

*Software*

The software architecture of the Power Subsystem (EPS) in satellite embedded systems is designed to efficiently manage power distribution, processing, and monitoring, while ensuring adaptability, scalability, and real-time operation. The system adopts a hybrid approach, combining Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) to achieve an optimal balance of flexibility, power efficiency, and system performance. This structure ensures that each software component is dedicated to specific tasks, making the system adaptable to varying conditions and ensuring reliable performance.

At the heart of the system lies the Data Acquisition Layer, which interfaces directly with the sensing hardware that collects telemetry data from key components across the satellite’s power system. This layer continuously gathers data on parameters like voltage, current, and temperature from critical components such as solar panels, batteries, and DC-DC converters. The raw data is filtered, normalized, and processed to ensure accuracy and readiness for making power management decisions. The Data Acquisition Layer is essential for providing reliable telemetry data and laying the foundation for real-time monitoring and decision-making.

Building on this foundation, the Monitoring and Protection Layer continuously compares the telemetry data with predefined operational thresholds. Its primary purpose is to protect the system by triggering protective actions when abnormal conditions, such as overvoltage, overcurrent, or overheating, are detected. For example, if a component exceeds its operational limits, the system may adjust power flow or shut down certain parts to prevent damage. The FPGA plays a crucial role in this layer by processing telemetry data in real time, enabling the satellite to quickly respond to conditions and make necessary adjustments without delay, thereby ensuring the stability of the power system.

The Optimization and Control Layer enhances the Power Subsystem by utilizing Model Predictive Control (MPC) algorithms. These algorithms predict future power demands, thermal behavior, and energy usage across the satellite, enabling proactive management of power resources. By forecasting future needs, the system can distribute energy efficiently across subsystems, optimizing the performance of the power system over time. The FPGA’s parallel processing capabilities allow it to handle multiple real-time tasks simultaneously, such as energy distribution, thermal regulation, and cell balancing, which improves overall efficiency and extends the satellite’s operational lifespan.

Communication between the Power Subsystem and other satellite subsystems is vital for coordinated operations. The Communication and Interface Layer ensures seamless data exchange between subsystems using communication protocols such as CAN bus or SpaceWire. The FPGA manages this communication, ensuring that critical updates, system status reports, and fault notifications are transmitted promptly, enabling timely interventions and adjustments.

The software execution within the Power Subsystem is optimized in a real-time operating environment, ensuring that critical tasks are completed within stringent time limits. The FPGA is responsible for handling time-sensitive tasks such as power regulation, sensor data collection, and protection functions. Its reprogrammable nature allows for flexibility in updates and improvements, making it an ideal choice for managing the dynamic and complex needs of satellite power systems. VHDL (VHSIC Hardware Description Language) is used to implement time-critical logic in the FPGA, enabling parallel processing and significantly enhancing system responsiveness. This capability allows the Power Subsystem to react swiftly to changing conditions, ensuring high reliability and performance.

The ASIC supports the system by handling fixed, low-power tasks such as voltage regulation and battery management. Since these tasks do not require reconfiguration, the ASIC is optimized for energy efficiency, helping to maintain the stability and cost-effectiveness of the satellite’s power system. By using the FPGA for dynamic, flexible tasks and the ASIC for stable, fixed operations, the Power Subsystem strikes an optimal balance between performance and efficiency, ensuring that the satellite operates effectively in space while minimizing energy consumption.

To validate the functionality of the Power Subsystem, a test bench was developed to simulate real-world conditions. The test bench facilitates waveform analysis, enabling the team to monitor the system’s behavior under various operational scenarios. This analysis helps identify potential performance issues such as voltage stability, response time, and power efficiency. By testing different configurations, the system can be fine-tuned for optimal performance before deployment, ensuring that the satellite is reliable throughout its mission.

1. FBGA

**The FPGA was utilized for real-time telemetry data processing, power distribution, and adaptive control, providing the system with the necessary flexibility to react to changing power demands in real time.**

The **FPGA** is an ideal choice for handling **real-time telemetry data processing** because of its parallel processing capabilities. This allows the **satellite power system** to simultaneously manage multiple input signals from the **solar panels**, **batteries**, and other critical power components, providing the flexibility to process large amounts of data quickly. The FPGA can adapt to changing conditions in the satellite’s power environment by adjusting the power distribution based on real-time feedback from various sensors. For example, when the satellite is exposed to fluctuating sunlight conditions or enters the Earth’s shadow, the FPGA can dynamically adjust the power output to subsystems, ensuring optimal energy utilization.

Additionally, the **adaptive control** provided by the FPGA enables real-time power regulation. By adjusting the distribution of power across subsystems, the FPGA helps maintain a consistent supply of energy to essential components such as **communication systems** and **onboard sensors**. This dynamic control minimizes the risk of power shortages and maximizes the satellite's overall efficiency. The ability to implement complex algorithms for **power management** and **fault detection** in hardware makes the FPGA a crucial element in meeting the **real-time** demands of satellite missions, where delayed responses could lead to significant operational risks.

1. **ASIC**

**The ASIC (Application-Specific Integrated Circuit) is specifically designed to handle fixed, essential tasks in the satellite's power subsystem, offering both low power consumption and high efficiency. Unlike the FPGA, which is reconfigurable and designed for dynamic functions, the ASIC is optimized for stable, non-changing operations. This specialization allows it to deliver consistent, high-performance results with minimal energy usage, making it an ideal solution for critical tasks like voltage regulation and battery management.**

**One of the primary responsibilities of the ASIC is voltage regulation, ensuring that each component of the satellite receives the correct voltage. This is crucial for preventing damage caused by power fluctuations, such as voltage surges or drops, which could otherwise compromise the satellite's subsystems. By maintaining stable voltage levels, the ASIC protects the satellite's delicate electronics and contributes to the overall longevity and reliability of the satellite's power system.**

**In addition to voltage regulation, the ASIC plays a vital role in battery management. It controls the efficient charging and discharging of the satellite's battery pack by regulating the voltage and current supplied to and from the battery. The ASIC helps extend the battery’s lifespan by preventing overcharging and overdischarging—conditions that can degrade battery performance over time. By managing these tasks with exceptional efficiency and low power consumption, the ASIC ensures that the satellite's power subsystem operates smoothly without unnecessarily draining the satellite’s energy resources. This low-power, high-efficiency approach helps optimize the overall energy consumption of the satellite, making the power system more reliable and sustainable for long-term space missions.**

| **Component** | **Role in Power Subsystem** | **Key Characteristics** | **Advantages** |
| --- | --- | --- | --- |
| **FPGA** | Real-time telemetry processing, adaptive power distribution, dynamic control | Reconfigurable, handles dynamic tasks, parallel processing | Flexibility, adaptability to changing power conditions, real-time data processing, rapid adjustments in power distribution |
| **ASIC** | Voltage regulation, battery management, fixed power control | Fixed function, low power consumption, optimized for specific tasks | High efficiency, stability, minimal energy consumption for stable tasks, ensures voltage consistency and battery longevity |

1. **Test bench**

**The test bench serves as a critical tool in the development of the Power Subsystem (EPS), enabling thorough simulation and verification of the satellite’s power management system before it is deployed into space. By using the test bench, the system can be subjected to a variety of operational scenarios, such as fluctuations in solar panel output, battery charge/discharge cycles, and changes in thermal conditions that might arise during different mission phases. These simulations provide invaluable insights into how the system responds to different power demands, helping to ensure that the FPGA and ASIC work together seamlessly to manage power distribution without failure.**

**Moreover, the test bench generates valuable waveform data that reflects how the power subsystem behaves in real-time. This data allows the design team to observe key factors like voltage stability, system response times, and overall efficiency. By analyzing these waveforms, potential issues—such as power spikes or inadequate power delivery to subsystems—can be identified early in the design process. This proactive approach enables the team to make the necessary adjustments to both hardware and software before the satellite is launched, ensuring that the power system is both reliable and resilient. Ultimately, the test bench ensures that the power subsystem is fully capable of handling the challenges of space missions, providing the reliability needed for successful satellite operations.**

**One of the standout advantages of using FPGA technology in the Power Subsystem is its ability to perform real-time data processing with minimal latency. Space missions demand immediate responses to telemetry data, particularly when managing power distribution. The FPGA’s parallel processing capabilities enable it to handle multiple power signals at once, reacting instantly to real-time telemetry data from sensors such as voltage, current, and temperature. This ability is crucial for ensuring that power flow adjustments—such as managing solar panel output, controlling battery charging, or regulating DC-DC converters—happen without delay.**

**The FPGA’s real-time processing is essential for maintaining the stability and efficiency of the power system, especially during the satellite’s orbit as it moves between areas of sunlight and Earth’s shadow. The FPGA dynamically adjusts the power flow to critical subsystems in real-time, ensuring that the satellite always receives a consistent power supply, regardless of changes in the satellite’s environment. Without the FPGA’s ability to make these immediate adjustments, the power system could face instability, potentially compromising the satellite’s mission. This real-time adaptability ensures that the satellite’s power subsystem remains functional and reliable throughout its mission, even in the face of changing conditions in space.**

1. **The Hybrid approach**

**Leveraging FPGA and ASIC technologies allows the satellite to operate with maximum power efficiency, quickly adapt to changing conditions, and maintain reliable performance throughout its mission.**

**The hybrid FPGA-ASIC approach is essential for the effective operation of the Power Subsystem (EPS) in satellite embedded systems. By combining the flexibility of FPGA with the efficiency of ASIC, this approach ensures the satellite can enjoy the benefits of both dynamic adaptability and energy savings. The FPGA is responsible for handling tasks that require real-time adjustments, such as dynamically distributing power and responding to fluctuating conditions like changes in solar power availability. Meanwhile, the ASIC takes care of fixed, critical operations, such as regulating voltage and managing the battery, ensuring stable and efficient performance.**

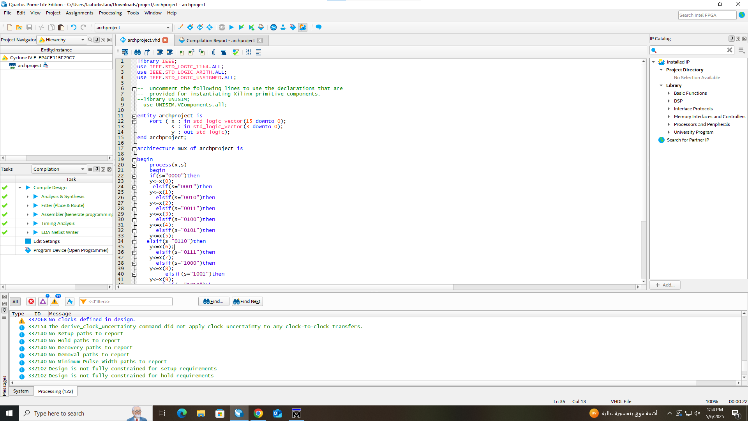
**This combination of FPGA and ASIC allows the satellite's power system to meet the demands of space by continuously adjusting to environmental shifts, such as changes in solar exposure and varying load conditions across the satellite’s subsystems. With the FPGA managing real-time power distribution and the ASIC handling power-efficient, stable operations, the satellite’s power system remains both flexible and efficient. This hybrid design ensures that the system optimizes power use, helping the satellite execute its mission without prematurely depleting its energy reserves, and ultimately ensuring operational reliability throughout the duration of the mission.**

# V. Simulation and observation

### **Observation and Simulation**

### The **Power Subsystem (EPS)** for satellite embedded systems requires precise control over power distribution and energy management to ensure reliable performance throughout the satellite's mission. In this research, a comprehensive **simulation** was conducted using **Midsim**, a simulation tool for **VHDL** code execution, to evaluate the performance of the **FPGA** and **ASIC** components. The primary objective was to test the system's ability to handle dynamic power distribution and validate its safety mechanisms under various operating conditions. The **VHDL code** written for the **FPGA** was designed to manage real-time telemetry data processing, while ASIC was responsible for **voltage regulation**, ensuring the stability and safety of the satellite's power system.

**Figure 6:** VHDL code for MUX



A screenshot of a computer

AI-generated content may be incorrect.

#### **Test Bench Setup**

#### The The simulation setup began by creating a detailed test bench environment within Midsim. This environment replicated the satellite’s Power Subsystem, including its components such as solar panels, battery storage, DC-DC converters, and the Power Distribution Module (PDM). The test bench was designed to provide input signals for power sources and simulate sensor feedback from various power system components, such as voltage, current, and temperature readings. The FPGA, responsible for processing these signals, was integrated into the test bench to handle real-time adjustments and power management.

#### The ASIC, in turn, was simulated to regulate the voltage levels within the power subsystem, ensuring that the satellite’s subsystems, including communication modules, onboard sensors, and payloads, received stable and reliable power. The test bench also included fault conditions to simulate overvoltage and overcurrent scenarios, ensuring that the protection mechanisms within the FPGA and ASIC could detect and respond to critical events.d simulate **sensor feedback** from various power s.

#### **Simulation Results**

#### Once the simulation was set up, the **Midsim** tool was used to run the **VHDL code**, producing **waveform results** that captured the behavior of the power system under varying conditions. These **waveforms** provided valuable insights into how the system responded to changes in energy generation and consumption. For example, the simulation showed how the system handled power fluctuations, particularly during transitions between the **solar panel's sunlight phase** and **eclipse periods**, where the **solar panels** no longer generated power, and the **battery system** took over to supply power.

A screenshot of a computer

AI-generated content may be incorrect.

#### The **FPGA's role** in the system was to dynamically adjust the power distribution based on real-time telemetry data. The simulation confirmed that the **FPGA** successfully managed **real-time telemetry processing**, responding to changes in the system's power requirements and maintaining the stability of the power flow throughout the satellite. The **ASIC**, on the other hand, was tasked with regulating the voltage supplied to various subsystems to ensure efficient operation. The simulation results demonstrated that the **ASIC** effectively managed the **voltage regulation**, preventing any power surges or dips that could damage sensitive subsystems.

#### **Waveform analysis** indicated that the power system could reliably manage power fluctuations, with the **FPGA** dynamically redistributing power when necessary. The **voltage stability** observed in the simulation was critical for ensuring that the satellite's subsystems received a constant and stable power supply, even during periods of fluctuating solar energy generation. Additionally, the **current monitoring system** in the simulation highlighted that the power subsystem could adapt to changing loads, efficiently powering the satellite’s equipment without causing overloads.

#### The simulation also tested the system’s ability to handle fault conditions, including **overvoltage** and **overcurrent**. In these scenarios, the **FPGA** responded promptly, triggering safety mechanisms to isolate the affected components and prevent damage to the satellite's subsystems. The **ASIC's safety features**, such as voltage regulation during extreme conditions, were validated in the simulation, confirming that the system could safely manage power supply under fault conditions.

#### **Accuracy and Performance**

#### The accuracy of the simulation was high, as the waveforms generated by **Midsim** matched expected theoretical values for power distribution and voltage regulation. By comparing the **simulation results** with theoretical predictions, we verified that the **FPGA** and **ASIC** components were performing as required. The system was able to respond to dynamic power demands and fluctuations without compromising stability or efficiency, confirming that the **FPGA and ASIC hybrid approach** was effective for satellite power subsystem management.

#### Furthermore, the simulation provided a platform for **iterative testing and refinement**. After analyzing the initial results, adjustments were made to optimize the performance of both the **FPGA** and **ASIC** components. For example, minor tweaks were made to the **FPGA's control logic** to ensure smoother transitions in power management, especially during sudden changes in **solar panel output**. These adjustments were re-tested in the simulation, further enhancing the power subsystem's responsiveness and efficiency.

#### **Prototyping and Safety Validation**

#### One of the key benefits of using Midsim for this simulation was the ability to test safety features and protection mechanisms without needing any physical hardware. The test bench setup in Midsim allowed us to simulate critical scenarios like overcurrent and overvoltage, helping us observe how the system would react to these extreme conditions. This kind of testing was essential to verify the built-in safety measures in the FPGA and ASIC, which are specifically designed to safeguard sensitive components from damage during such events. The simulation results proved that the protection circuits worked as intended, successfully isolating affected components and allowing the satellite to continue functioning smoothly.

#### The use of Midsim also provided an invaluable opportunity to thoroughly test the hybrid FPGA-ASIC approach. It gave us detailed data to confirm the system's performance under different conditions. The simulation’s accuracy and its ability to adjust to real-time changes in data without delay made it clear that the FPGA and ASIC hybrid model would deliver reliable, efficient power management for satellite systems. This comprehensive testing confirmed that the system is both robust and adaptable, ensuring the satellite can handle a variety of challenging scenarios in space with ease.

### **Results**

### The **simulation results** were obtained using **Midsim**, where the **VHDL code** for the **satellite power subsystem** was applied and tested under various conditions. The **test bench** in **Midsim** simulated real-world conditions, allowing us to evaluate the performance of the **FPGA** and **ASIC** components in managing **power distribution**, **voltage regulation**, and **telemetry processing** for the satellite's power subsystem.

### The **FPGA** was responsible for real-time data processing, adjusting the power flow based on the telemetry data from the **solar panels**, **battery systems**, and **DC-DC converters**. The **ASIC** handled the more fixed tasks, ensuring **voltage regulation** and stable power delivery to the satellite's subsystems. The **simulation** showed that the **FPGA** dynamically managed the power distribution based on fluctuations in solar exposure and battery charge levels, while the **ASIC** provided efficient and stable voltage regulation for sensitive components.

### The **waveforms** generated during the simulation provided a clear representation of how the system responded to varying input conditions. These results confirmed that the **VHDL-implemented power subsystem** functioned as expected, with no voltage dips or surges, ensuring reliable and efficient power management. The **FPGA's adaptability** and **ASIC's efficiency** were validated, showing that the hybrid approach could effectively manage dynamic changes in power demand while maintaining system stability.

# VI. Key Themes and Analysis Embedded Satellite Systems: FPGA vs. ASIC

1. Radiation Tolerance and Reliability

Radiation tolerance is a critical factor when designing embedded systems for space applications. In the harsh environment of space, electronic components are constantly exposed to high levels of radiation, which can cause significant damage to the systems. This exposure can lead to single-event upsets (SEUs), total ionizing dose (TID) degradation, and latch-up effects, all of which threaten the reliability and longevity of the satellite’s electronics. As such, choosing between FPGAs and ASICs for space missions requires careful consideration of their ability to withstand these radiation hazards.

ASICs, when designed using Radiation-Hardened by Design (RHBD) methodologies, offer robust radiation resilience. These ASICs are built with features such as triple-well isolation, error correction mechanisms, and latch-up protection, all of which enhance their ability to perform reliably in the extreme conditions of space. This makes them ideal for critical systems where long-term stability and dependability are essential. With these built-in safeguards, RHBD ASICs provide a high level of reliability, making them the preferred choice for many space applications where radiation hardness is a top priority.

On the other hand, radiation-hardened FPGAs, like the Xilinx Virtex-5QV and Microsemi RTG4, have been specifically designed to endure the radiation levels found in space. While they are more radiation-resistant than commercial FPGAs, these hardened FPGAs often fall short in processing power and efficiency compared to their commercial counterparts. The trade-off for their enhanced radiation tolerance is a slight compromise in their overall performance and processing capability, which must be considered when selecting the right solution for space-based missions.

For low Earth orbit (LEO) missions, Commercial-Off-The-Shelf (COTS) FPGAs can be used effectively, provided that adequate shielding and redundancy techniques are implemented. In these environments, the risk of radiation damage is lower, and with proper protection, COTS FPGAs can offer an efficient, cost-effective solution for certain mission requirements. However, for more critical or high-radiation environments, more resilient, radiation-hardened components like RHBD ASICs or radiation-hardened FPGAs are essential to ensure reliable and continuous operation.

The choice between ASICs, radiation-hardened FPGAs, and COTS FPGAs ultimately depends on the specific mission requirements, balancing performance, cost, and radiation tolerance to ensure the success of space operations.

* Case Studies:
* Bensikaddour et al. implemented a chaos-based encryption scheme on an FPGA while integrating Triple Modular Redundancy (TMR) to counteract SEU vulnerabilities.
* Rapuano et al. evaluated Myriad 2-based AI accelerators vs. FPGA solutions for short-duration LEO missions, showing that COTS FPGAs, when shielded, can meet mission reliability standards.

1. Performance and Power Efficiency

The efficiency of space computing is primarily determined by performance-per-watt, as satellites operate under tight power constraints while simultaneously handling demanding computational tasks, including AI inference, cryptography, and hyperspectral imaging. In such power-limited environments, every bit of energy must be used efficiently to ensure the satellite remains operational throughout its mission.

FPGAs offer a unique advantage in this area due to their fine-grained parallelism, which enables them to provide high throughput for tasks that require real-time processing, such as AI inference, image recognition, and signal processing. This parallelism allows FPGAs to efficiently handle multiple tasks simultaneously, making them ideal for computationally intensive workloads that need to process data in real-time. While FPGAs are excellent at providing flexible and scalable performance, they tend to consume more power than ASICs. However, their power consumption can be optimized by employing low-power architectures and dynamic scaling techniques, which help balance performance and energy efficiency, especially in non-peak operational phases.

On the other hand, ASICs, when mass-produced, offer superior energy efficiency compared to FPGAs. They are custom-designed for specific tasks, and as a result, they can deliver higher processing power while consuming less energy for fixed-function operations. This makes ASICs particularly well-suited for tasks that don’t require the flexibility of an FPGA, such as performing repetitive operations in cryptography or image processing. ASICs’ specialized nature allows them to maximize energy efficiency, delivering significant gains in power-per-watt performance for dedicated tasks.

In essence, while FPGAs generally consume more power due to their reconfigurability and versatility, their ability to optimize power consumption through architectural design and dynamic adjustments makes them suitable for complex, variable tasks. ASICs, with their fixed functionalities, excel in energy efficiency for tasks that don’t require constant reconfiguration, making them ideal for missions where energy efficiency is paramount. Balancing the strengths of both technologies allows space systems to achieve the best combination of performance, power efficiency, and flexibility.

* Case Studies:
* Rapuano et al. (CloudScout Mission) found that FPGA-based AI inference was 2.4× faster than Myriad 2 VPU but also had 1.8× higher power consumption.
* Lentaris et al. demonstrated that FPGAs achieved the best GFLOPS/W ratio among embedded CPUs, DSPs, and GPUs, proving superior for real-time spacecraft navigation.

1. Reconfigurability and Upgradability

For long-term satellite missions, hardware flexibility becomes a vital advantage, especially in the face of evolving mission requirements and the need for system updates over time. FPGAs offer the unique benefit of post-launch reconfigurability, allowing software-defined updates to be made to critical systems such as AI models, encryption protocols, and onboard decision-making algorithms. This flexibility ensures that the satellite can adapt to new challenges, incorporate updated AI models, or implement enhanced encryption protocols, all without the need for a costly and complex hardware upgrade. The ability of FPGAs to adjust in real-time to changing mission demands makes them indispensable for autonomous satellites that rely on evolving AI algorithms to improve decision-making and optimize performance over the course of the mission.

Unlike FPGAs, ASICs are fixed once fabricated, which makes them an excellent choice for tasks that require consistent, reliable performance but limits their usefulness for missions that demand continuous updates or adaptability. Since ASICs cannot be reprogrammed after production, they are best suited for fixed tasks such as sensor processing or power regulation, where their efficiency and energy savings outweigh the need for flexibility. However, this inherent lack of reconfigurability makes them less ideal for missions requiring ongoing software updates or those that might face unforeseen challenges that demand system changes.

To bridge the gap between the flexibility of FPGAs and the efficiency of ASICs, reconfigurable System on Chips (SoCs) like the Xilinx Zynq UltraScale+ have emerged. These advanced systems combine the reconfigurable FPGA fabric with embedded CPUs, enabling dynamic acceleration of specific tasks such as AI inference and cryptographic functions. This hybrid approach allows satellites to not only adapt in real-time to new demands but also optimize critical computational tasks in a power-efficient manner. By leveraging both FPGA and CPU capabilities in a single device, reconfigurable SoCs offer the best of both worlds—flexibility and efficiency—making them ideal for long-term space missions where both adaptability and performance are crucial.

* Case Studies:
* Guesmi et al. showcased partial FPGA reconfiguration for cryptographic security, allowing real-time encryption updates to mitigate evolving cybersecurity threats.
* NASA and ESA deep-space missions increasingly integrate FPGA-based AI accelerators, allowing for software-defined feature extraction, fault detection, and spacecraft autonomy.

1. Development Cost, Complexity, and Time-to-Market

The economic feasibility of satellite missions is heavily influenced by development costs, design complexity, and the pressure of meeting tight time-to-market constraints. ASICs, while offering exceptional power efficiency and performance for fixed tasks, come with high non-recurring engineering (NRE) costs due to the custom fabrication processes involved. These upfront costs make ASICs more suitable for high-volume satellite constellations where the investment in custom hardware can be justified by economies of scale. However, the high NRE costs mean that ASICs are often not a viable option for smaller, one-off satellite missions, where cost-efficiency is a primary concern.

FPGAs, on the other hand, offer a more flexible and cost-effective solution for satellite missions, especially for small-scale or experimental projects. Although FPGAs typically have higher per-unit costs compared to ASICs, their ability to reduce design risk and accelerate prototyping makes them a highly attractive option for missions that require quick turnaround times or where design iterations may be necessary. With FPGAs, satellite developers can quickly adapt to changes or unforeseen issues, making them ideal for rapid prototyping and low-volume production. This flexibility allows for faster deployment of satellite systems, particularly in missions that are experimental or involve new technologies.

Time-to-market is another critical factor in satellite mission planning, and here, FPGA-based systems offer a significant advantage. FPGAs can be rapidly deployed and reprogrammed as needed, allowing for quick iterations and faster system validation. In contrast, the development cycle for ASICs is far longer, as it involves time-consuming custom design, fabrication, and testing processes. This extended timeline can significantly delay mission schedules, making ASICs less attractive for missions with tight deadlines or when rapid deployment is essential. By reducing design time and offering adaptability throughout the mission lifecycle, FPGA-based systems enable faster, more flexible satellite missions that can be adjusted in real-time as new challenges arise.

* Case Studies:
* Guesmi et al. used High-Level Synthesis (HLS) for FPGA-based AI cryptographic pipelines, reducing development complexity and time-to-deployment.
* Lentaris et al. observed that NASA and ESA space missions frequently rely on FPGAs for early-stage testing, as prototyping on FPGA platforms is significantly faster than developing an ASIC.

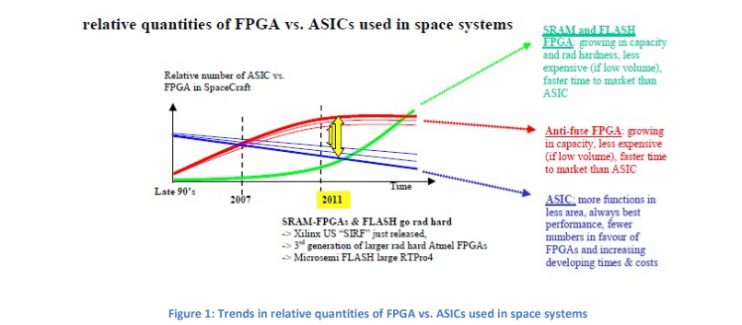
# ***VII. Challenges and Future Trends***

The Power Subsystem (EPS) in satellite embedded systems, particularly when employing a hybrid FPGA-ASIC approach, presents several challenges that must be overcome to ensure optimal performance. One of the primary challenges is the dynamic nature of satellite power systems, where power availability can fluctuate due to varying solar exposure, battery charge levels, and shifting operational loads. Managing these fluctuations in real-time while maintaining safe and efficient operation remains a critical task. Even with the reconfigurability of FPGAs, achieving seamless integration between the FPGA and ASIC to manage power distribution and voltage regulation dynamically—without sacrificing efficiency—continues to be an ongoing challenge. Ensuring that these two technologies work in harmony to maintain power stability across different mission phases is crucial for the satellite's performance.

Another significant challenge arises when managing power under fault conditions such as overvoltage, overcurrent, and thermal overloads. While the system is designed to respond to these anomalies, the complexity lies in ensuring that both the FPGA and ASIC can handle real-time fault detection and corrective actions efficiently. The protection mechanisms must be both robust and responsive, adapting to rapidly changing conditions to maintain the satellite’s operational integrity. This requires designing a system that can respond immediately to faults without causing system downtime or data loss. Managing these conditions in real-time, especially in the extreme environments of space, requires intricate design and careful consideration of how the FPGA and ASIC can collaborate to ensure the satellite’s survival under stress.

In addition, Figure 3 provides a visual representation of the shifting trends in FPGA versus ASIC usage in space systems. The graph illustrates how the adoption of FPGAs has increased over time, in contrast to ASICs, which remain more dominant in high-performance, fixed-function tasks. This shift is significant as it highlights the growing versatility and reconfigurability of FPGAs, which are becoming increasingly well-suited for modern satellite missions. These missions often require flexibility, adaptability, and the ability to process data in real-time—capabilities that FPGAs excel in. With their capacity to be reprogrammed post-launch, FPGAs allow for future-proofing of satellite systems, giving them the flexibility to adjust to new mission requirements or unforeseen challenges.

**Figure 3:** Trends in Relative Quantities of FPGA vs. ASICs Used in Space Systems [18]

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1. Shift from ASICs to FPGAs Over Time:

In the late 1990s, ASICs dominated the space industry due to their performance and reliability, particularly in mission-critical applications where stability and power efficiency were paramount. However, as satellite missions became more complex and the need for reconfigurable hardware grew, the trend began shifting toward FPGAs.

By 2007, the increased capacity, radiation tolerance, and flexibility of FPGAs made them an attractive alternative to ASICs. The ability of FPGAs to be reprogrammed even after launch provided an important advantage, especially for long-duration missions where adaptability is crucial.

By 2011, SRAM-based and Flash-based FPGAs had significantly advanced, leading to further reduction in the reliance on ASICs. FPGAs could now offer comparable or even superior performance in many space applications while remaining cost-effective, especially for low-volume production. This advancement significantly influenced the adoption of FPGAs in satellite systems.

1. Different FPGA Technologies and Their Growth: SRAM and Flash FPGAs (Green Line):

These FPGA types have seen substantial growth in capacity and radiation hardness, making them increasingly viable for use in space missions. Notably, SRAM-based FPGAs offer high reconfigurability and low latency, while Flash-based FPGAs provide non-volatile memory, which is essential for maintaining configuration during power-down scenarios.

The increasing performance and cost-effectiveness of these technologies have enabled rapid time-to-market compared to ASICs, especially for small and medium-scale missions. They are ideal for applications that require a flexible and scalable design but do not have the same high-volume production requirements as traditional ASICs.

Examples of such FPGAs include Xilinx’s SRAM-based US “SRF” series, Atmel rad-hard FPGAs, and Microsemi’s Flash-based RT Pro4, all of which have found extensive use in space-based applications, ranging from AI processing to signal processing in satellite systems.

1. Anti-fuse FPGAs (Red Line):

Anti-fuse FPGAs are also growing in adoption due to their cost-effectiveness in low-volume production scenarios. These FPGAs are one-time programmable, which makes them an attractive option for long-life missions where the hardware design does not require post-launch updates.

While Anti-fuse FPGAs are not as flexible as SRAM-based or Flash-based FPGAs, they offer a reliable solution for systems that require a fixed functionality once deployed, making them suitable for low-cost and low-risk applications where the system does not need to be reprogrammed after deployment.

1. ASICs Remain in Niche High-Performance Applications (Blue Line):

ASICs still play a vital role in high-performance, mission-critical applications where the highest performance per watt and maximum reliability are essential. These custom-built chips are optimized for specific tasks, making them particularly useful in extreme space conditions, such as deep-space exploration and scientific experiments onboard satellites.

However, despite their advantages, ASICs face limitations when compared to FPGAs in terms of flexibility and time-to-market. The longer development cycles and high non-recurring engineering (NRE) costs associated with ASIC development make them less suited for satellites that require adaptability and frequent updates, especially in smaller missions.

ASICs remain dominant in radiation-hardened applications that require absolute reliability and efficiency, such as sensitive instruments, data acquisition systems, or long-term space missions where performance cannot be compromised. However, the growing use of FPGA technology for more flexible, dynamic, and scalable applications in satellites is challenging the prevalence of ASICs.

Another challenge is optimizing the **real-time adaptability** of the system. As satellite missions become more complex, the ability of the **FPGA** to process increasing amounts of telemetry data in real time, while maintaining **voltage stability** and managing power distribution, becomes even more crucial. The complexity of processing and the need to maintain reliable operation across multiple power subsystems require further advancements in **parallel processing** and **hardware design** to improve **efficiency** and **responsiveness**.

Looking toward the **future**, the development of **more efficient power storage systems** and **advanced energy management technologies** will likely be a game-changer in satellite power subsystems. **Solid-state batteries**, **supercapacitors**, and next-generation **energy storage solutions** offer promising alternatives to traditional **lithium-ion batteries**, with better **energy density**, **faster charging times**, and improved **thermal management**. These innovations could significantly extend the operational lifetimes of satellites, enabling longer missions in space without the need for recharging or re-supply.

In terms of **FPGA and ASIC technologies**, future trends point to **miniaturization** and **higher integration** of these devices, making them even more **power-efficient** while maintaining or improving their performance. Advances in **multi-core FPGA architectures** will allow for faster data processing and the ability to handle even larger telemetry data streams. Additionally, the **use of AI and machine learning** in **predictive power management** will become more prevalent, allowing satellites to better anticipate power demands and optimize the distribution of resources in real-time. **AI algorithms** will enable satellites to **predict energy needs**, **adjust power consumption patterns**, and even **balance loads** across different subsystems before issues arise, ultimately enhancing the efficiency and lifespan of the satellite.

Furthermore, the increased focus on **autonomous satellites** means that **power subsystems** will need to integrate with **autonomous navigation** and **communication systems** that function seamlessly without human intervention. For this, the **FPGA and ASIC approach** will need to evolve to accommodate **smart power management algorithms** that can adjust based on **mission-critical requirements**, such as **positioning** or **sensor data collection**, and environmental factors like **solar exposure** or **temperature** variations.

### **Conclusion**

In conclusion, the hybrid FPGA-ASIC approach offers a highly efficient and reliable solution for managing the Power Subsystem (EPS) in satellite embedded systems. This research has showcased how the integration of FPGA and ASIC components can handle both real-time dynamic control and fixed, low-power tasks, ensuring optimal power distribution and voltage regulation across satellite subsystems. Through VHDL code and simulation using Midsim, we have validated the performance of both components, confirming their capability to manage power distribution efficiently and maintain system stability under a variety of operational conditions.

The simulation results confirmed that the FPGA could handle real-time telemetry processing effectively, while the ASIC ensured consistent voltage regulation across the satellite’s systems. Moreover, safety features such as overvoltage and overcurrent protection were successfully validated, confirming that the power subsystem would operate safely even during faulty conditions. The hybrid FPGA-ASIC approach proved to be an effective strategy in achieving both real-time adaptability and energy efficiency, allowing the satellite to respond to fluctuating power conditions while maintaining operational stability.

Looking ahead, several future trends hold the potential to enhance the performance and reliability of satellite power subsystems. Innovations in AI-driven control, advanced energy storage solutions, and the miniaturization of FPGA/ASIC components will play key roles in optimizing power distribution, load balancing, and fault management in upcoming satellite missions. As satellite missions become more complex, the need for smarter, autonomous power systems capable of adjusting to real-time operational demands will only increase. The hybrid FPGA-ASIC approach will undoubtedly continue to be at the forefront of these innovations, enabling more advanced and adaptive power systems.

Ultimately, this research highlights the effectiveness of the hybrid FPGA-ASIC approach in addressing the operational demands of satellite power subsystems. With ongoing advancements in simulation tools, hardware design, and AI-powered optimization, the future of satellite power management looks promising, offering improved efficiency, greater reliability, and higher mission success rates. The continued development of these technologies ensures that satellite systems will be better equipped to handle the increasing complexity and evolving needs of space missions.

# References

[1] R. Amdouni et al., "FPGA Implementation of Robust and Secure Transmission Cryptosystem for Satellite Images," in IEEE Access, vol. 12, pp. 115561-115587, 2024, doi: 10.1109/ACCESS.2024.3444732.

[2] Rapuano, E.; Meoni, G.; Pacini, T.; Dinelli, G.; Furano, G.; Giuffrida, G.; Fanucci, L. An FPGA-Based Hardware Accelerator for CNNs Inference on Board Satellites: Benchmarking with Myriad 2-Based Solution for the CloudScout Case Study. *Remote Sens.* 2021, *13*, 1518.3. <https://doi.org/10.3390/rs13081518>

[3] Ekblad, A. (2023). *Accelerating Machine Learning Inference for Satellite Component Feature Extraction Using FPGAs* (Master's thesis). Florida Institute of Technology. Retrieved from <https://repository.fit.edu/etd/1396/>​

[4] Rapuano, E., Meoni, G., Pacini, T., Dinelli, G., Furano, G., Giuffrida, G., & Fanucci, L. (2021). An FPGA-based hardware accelerator for CNNs inference on board satellites: Benchmarking with Myriad 2-based solution for the CloudScout case study. *Remote Sensing, 13*(8), 1518. <https://doi.org/10.3390/rs13081518>

[5] ​Ekblad, A., Mahendrakar, T., White, R. T., Wilde, M., Silver, I., & Wheeler, B. (2023). Resource-constrained FPGA design for satellite component feature extraction. *2023 IEEE Aerospace Conference (AERO)*. <https://arxiv.org/abs/2301.09055>​

[6] Diana, L., & Dini, P. (2024). Review on hardware devices and software techniques enabling neural network inference onboard satellites. *Remote Sensing, 16*(21), 3957. <https://doi.org/10.3390/rs16213957>

[7] Lentaris, G., Maragos, K., Stratakos, I., Papadopoulos, L., Papanikolaou, O., Soudris, D., Lourakis, M., Zabulis, X., Gonzalez-Arjona, D., & Furano, G. (2018). High-performance embedded computing in space: Evaluation of platforms for vision-based navigation. *Journal of Aerospace Information Systems, 15*(4), 178–192. <https://arc.aiaa.org/doi/10.2514/1.I010555>

[8] GeeksforGeeks. (n.d.). *FPGA vs ASIC – What are the Differences?* Retrieved from <https://www.geeksforgeeks.org/fpga-vs-asic/>

[9] Matiieshyn, P. (2023, October 6). *ASIC vs FPGA: A Comparison of Hardware Solutions*. Lemberg Solutions. Retrieved from <https://lembergsolutions.com/blog/asic-vs-fpga-comparison-hardware-solutions>

[10] El-Latif, A. A. A., Abd-El-Atty, B., Abd-El-Latif, A. A., & Venkatraman, S. (2023). FPGA implementation of robust and secure transmission cryptosystem for satellite images. *IEEE Transactions on Aerospace and Electronic Systems*. <https://doi.org/10.1109/TAES.2023.10638129>​

[11] ​Arimoto, M., Harita, S., Sugita, S., Yatsu, Y., Kawai, N., Ikeda, H., Tomida, H., Isobe, N., Ueno, S., Mihara, T., Serino, M., Kohmura, T., Sakamoto, T., Yoshida, A., Tsunemi, H., Hatori, S., Kume, K., & Hasegawa, T. (2017). Development of a 32-channel ASIC for an X-ray APD detector onboard the ISS. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*. <https://doi.org/10.1016/j.nima.2017.09.003>

[12] ​FPGAkey. (2020, November. *Learn the difference between FPGA and ASIC in 15 minutes*. FPGAkey. Retrieved from <https://www.fpgakey.com/technology/details/difference-between-fpga-and-asic>

[13] S. Bose, M. Bhuyan, and R. S. D. Wahidabanu, "A formal technique for hardware interface design," ResearchGate, [Online]. Available: <https://www.researchgate.net/publication/3325107_A_formal_technique_for_hardware_interface_design>

[14] N. Ramos, Design of the Electrical Power Subsystem for a University CubeSat, M.S. thesis, Instituto Superior Técnico, University of Lisbon, 2018. [Online]. Available: <https://istsat-one.tecnico.ulisboa.pt/~istsat-one.daemon/docs/thesis_NunoRamos_EPS_2018.pdf>

[15] B. Martin, "Shrinking communication satellite subsystems," EDN Network, May 2019. [Online]. Available: <https://www.edn.com/shrinking-communication-satellite-subsystems/>

[16] M. Ramezanpour, "Hybrid ASIC-FPGA Flow," ResearchGate, 2023. [Online]. Available: <https://www.researchgate.net/figure/Hybrid-ASIC-FPGA-Flow_fig3_372199463>

[17] C. Chen, "FPGA vs ASIC: Which is better?" DEV Community, Oct. 2022. [Online]. Available: <https://dev.to/carolineee/fpga-vs-asic-which-is-better-43pb>

[18] D. Boada, Development of an Electrical Power System for a CubeSat Mission, European Space Agency, 2015. [Online]. Available: <https://amstel.estec.esa.int/tecedm/website/stag_ygt/Boada.pdf>